10-19-00

A

Patent Application Transmittal

(only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Correspondence Address:
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Date: October 18, 2000
Attorney Docket No.: 450117-02749

ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Sir:

With reference to the filing in the United States Patent and Trademark Office of an application for patent in the name(s) of:

Jens WILDHAGEN

entitled:

DIGITAL STEREO DEMULTIPLEXER

The following are enclosed:

- X Specification (10 pages)
- X 5 Sheet(s) of Drawings
- X 9 Claim(s) (including 1 independent claim(s))
- ___ This application contains a multiple dependent claim

- X Our check for $ 710.00, calculated on the basis of the claims as amended by any enclosed preliminary amendment as follows:

Basic Fee, $710.00 ($355.00)	$ 710.00
Number of Claims in excess of 20 at $18.00 ($9.00) each:	-0-
Number of Independent Claims in excess of 3 at $80.00 ($40.00) each:	-0-
Multiple Dependent Claim Fee at $270.00 ($135.00)	-0-
Total Filing Fee	$ 710.00

- ___ Assignment Recording Fee $40.00 -0-

- X Oath or Declaration and Power of Attorney
  - X New ___ signed X unsigned
  - ___ Copy from a prior application (37 C.F.R. 1.63(d))

- X Certified copy of each of the following application(s) to substantiate the claim(s) for priority made in the Declaration:

Application No.	Filed	In
99 120 798.6	20 October 1999	Europe

Please charge any additional fees required for the filing of this application or credit any overpayment to Deposit Account No. 50-0320.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicant

By: William S. Frommer
Reg. No. 25,506

FROMMER LAWRENCE & HAUG LLP
745 FIFTH AVENUE NEW YORK, NEW YORK 10151

October 18, 2000

Assistant Commissioner for Patents
Washington, D.C. 20231

Re: U.S. Patent Application
Applicant: Jens WILDHAGEN
Our Ref.: 450117-02749

Dear Sir:

Enclosed are papers constituting the above patent application which is being filed under 37 C.F.R. 1.53 without a signed Declaration. Please accord a filing date and a serial number to such application and inform the undersigned thereof so that a signed Declaration and the surcharge required by 37 C.F.R. 1.16(e) may be duly filed.

Please address all correspondence to:

William S. Frommer, Esq.
FROMMER LAWRENCE & HAUG LLP
745 Fifth Avenue
New York, New York 10151

Respectfully,

William S. Frommer
Reg. No. 25,506
Attorney for Applicant
Enclosures

J:\SONY\02749\53BAPUNS.EXM (WSF:sa)

PATENT
450117-02749

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Jens WILDHAGEN

Filed : Herewith

For : DIGITAL STEREO DEMULTIPLEXER

745 Fifth Avenue
New York, New York 10151
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EXPRESS MAIL

Mailing Label Number EL588273212US

Date of Deposit October 18, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" Service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Edward May
(Typed or printed name of person mailing paper or fee)

(Signature of person mailing paper or fee)

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Before the issuance of the first Official Action, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims as follows:

Claim 3, line 1, delete "or 2";

Claim 8, line 1, delete "or 7";

Claim 9, line 1, delete "anyone of claims 6 to 8" and insert --claim 6--.

REMARKS

The claims have been amended to eliminate multiple dependencies. The filing fee has been calculated based upon these amendments to the claims.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicant

By: _____
William S. Frommer
Reg. No. 25,506
Tel. (212) 588-0800

PATENT
450117-02749

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

TITLE: DIGITAL STEREO DEMULTIPLEXER

INVENTOR: Jens WILDHAGEN

William S. Frommer
Registration No. 25,506
FROMMER LAWRENCE & HAUG LLP
745 Fifth Avenue
New York, New York 10151
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Description

The present invention relates to the demultiplexing of a frequency demodulated stereo-multiplex signal.

In fm-broadcasting a stereo-multiplex signal is frequency modulated. The stereo-multiplex signal consists of a stereo-sum signal and a stereo-difference signal. The stereo-difference signal is amplitude modulated with suppressed carrier. To allow a coherent amplitude demodulation of the stereo-difference signal at the receiver, a pilot carrier with half the AM-carrier frequency is added to the stereo-multiplex signal.

The stereo-sum signal and the stereo-difference signal are defined by

$$m_s(t) = a_l(t) + a_r(t)$$
$$m_d(t) = a_l(t) - a_r(t)$$

wherein $a_l(t)$ is the signal of the left audio channel and $a_r(t)$ is the signal of the right audio channel.

The stereo-multiplex signal is defined by

$$m_{stmux}(t) = m_s(t) + \sin(2\,\omega_{pil}t) \cdot m_d(t) + A_{pil} \cdot \sin(\omega_{pil}t)$$

wherein ω_{pil} is the carrier frequency and A_{pil} is the amplitude of the carrier.

The stereo-multiplex signal is frequency modulated:

$$S_{FM}(t) = A_{FM}\cos\left(\omega_c(t) + \Delta\omega \int_{-\infty}^{t} m_{stmux}(\tau)\, d\tau\right)$$

with ω_c: carrier frequency

$\Delta\omega$: frequency deviation

At the receiver side the frequency modulated stereo-multiplex signal is frequency demodulated and stereo-demultiplexed to calculate the left and right

audio signal.

For the stereo demultiplexing, the stereo demultiplexer needs to recover the 2nd harmonic of the pilot carrier. Therefore, the pilot carrier is separated from the frequency demodulated stereo-multiplex signal m(t) by a bandpass filter and a PLL locks to the separated pilot carrier and generates the 2nd harmonic of the pilot carrier. The 2nd harmonic, that is locked in phase to the pilot carrier is needed for the coherent amplitude demodulation of the stereo-difference signal.

Figure 3 shows the basic functionality of a state of the art stereo demultiplexer. The received frequency modulated stereo-multiplex signal $S_{FM}(t)$ is input to a frequency demodulator 17. The frequency demodulator 17 outputs the frequency demodulated stereo-multiplex signal m(t) that corresponds to the stereo-multiplex signal $m_{stmux}(t)$ as generated on the transmitter side. On basis of this stereo-multiplex signal m(t) a PLL-circuit 19 with preceding bandpass filter 18 generates the 2nd harmonic of the pilot carrier, i. e. a signal $2\cdot\sin(2\omega_{pil}t)$, which is needed for the coherent amplitude demodulation of the stereo-multiplex signal m(t) to gain the stereo-difference signal $m_d(t)$.

The coherent amplitude demodulation is performed by way of a demodulator 1 which receives the stereo-multiplex signal m(t) at its first input and the 2nd harmonic of the pilot carrier at its second input. The output signal of the demodulator 1 is input to a filter 20 which outputs the stereo-difference signal $m_d(t)$.

The stereo-sum signal $m_s(t)$ is generated by a lowpass filtering of the stereo-multiplex signal m(t) with a lowpass filter 21 that receives the output signal of the frequency demodulator 17.

The left audio signal is calculated by an addition of the stereo-sum signal $m_s(t)$ and the stereo-difference signal $m_d(t)$ with an adder 3. The right audio signal r(t) is calculated by a subtraction of the stereo-difference signal $m_d(t)$ from the stereo-sum signal $m_s(t)$ with a subtracter 6.

Therefore, the stereo-sum signal $m_s(t)$ is generated by a lowpass filtering of the stereo-multiplex signal m(t) and the stereo-difference signal $m_d(t)$ is generated by a coherent amplitude demodulation of the amplitude modulated stereo-difference signal. The left and right audio signals l(t) and r(t) are calculated by addi-

tion and subtraction of the stereo-sum signal and the stereo-difference signal:

$$r(t) = m_s(t) - m_d(t) = (a_l(t) + a_r(t)) - (a_l(t) - a_r(t)) = 2a_r(t)$$
$$l(t) = m_s(t) + m_d(t) = (a_l(t) + a_r(t)) + (a_l(t) - a_r(t)) = 2a_l(t)$$

In a digital frequency demodulator the frequency demodulation needs to be performed at a high sampling rate because the bandwidth of the frequency modulating signal is about

$$B_{fm} = 2(\Delta F + 2f_{nf})$$

with ΔF being the frequency deviation and f_{nf} being the modulation frequency.

From this equation follows that the bandwidth of the frequency modulating signal is much larger than the bandwidth of the modulating signal. Therefore, the frequency demodulated signal can be sampling rate decimated.

Furtheron, the bandwidth of the stereo-multiplex signal is larger than the bandwidth of the audio signal. This can easily be seen in the above equation which defines the stereo-multiplex signal $m_{stmux}(t)$. Therefore, the sampling rate can be reduced in the stereo demultiplexer.

The digital stereo demultiplexer shown in Fig. 4 differs to that shown in Fig. 3 in that the filter 20 and the lowpass filter 21 are replaced by a first sampling rate decimation filter 22 which comprises a digital filter for the generation of the stereo-difference signal $m_d(t)$ and a second sampling rate decimation filter 23 which comprises a digital lowpass filter for the generation of the stereo-sum signal $m_s(t)$. Both sampling rate decimation filters have a decimation factor of D.

This solution has the disadvantage that the DPLL 19, which works similar to the PLL 19 shown in Fig. 3, needs to run at a high sampling rate. This requires high calculation power and therefore a high power consumption of the DSP that realizes the stereo demultiplexer.

The DPLL can also work at a reduced sampling rate. A simple method is to reduce the sampling rate of the bandpass filter output signal and to

interpolate the DPLL output signal.

Fig. 5 shows such a digital stero-demultiplexer comprising a digital PLL-circuit 25 which works at a reduced sampling rate. In this stereo demultiplexer the generation of the stereo-difference signal $m_d(t)$ and the stereo-sum signal $m_s(t)$ is identical as in the stereo demultiplexer shown in Fig. 4, only the generation of the 2nd harmonic of the pilot carrier differs.

The bandpass filter 18 shown in Figs. 3 and 4 is replaced with a third sampling rate decimation filter 24 which comprises a digital bandpass filter. The third sampling rate decimation filter 24 has a sampling rate decimation factor E. The DPLL 25 works with the reduced sampling rate and therefore receives the output signal of the third sampling rate decimation filter 24.

The coherent amplitude demodulation of the stereo-difference signal $m_d(t)$ needs to be performed at a sampling rate which is higher than the sampling rate of the audio signal, since the bandwidth of the stereo-multiplex signal m(t) is higher than the bandwidth of the audio signal. Therefore, the carrier for the coherent amplitude demodulation of the stereo-difference signal $m_d(t)$ needs to be generated with a higher sampling rate.

Fig. 5 shows that the output signal of the digital PLL-circuit 25 is interpolated in an interpolation unit 26 with an interpolation factor of E so that the 2nd harmonic of the carrier is generated with a sampling rate that equals to the sampling rate of the stereo-multiplex signal m(t). Thereafter, to perform the coherent amplitude demodulation which is necessary to generate the stereo-difference signal $m_d(t)$, the so generated carrier with a carrier frequency of $2\omega_{pil}$ that is locked in phase to the pilot carrier is multiplied with the stereo-multiplex signal m(t) by the demodulator 1.

In this embodiment the DPLL 25 runs at a reduced sampling rate and therefore outputs a lower number of samples per sample of the stereo-multiplex signal than the DPLL 19 shown in Fig. 4. So the required calculation power is low. On the other hand, the decimation bandpass filter within the third sampling rate decimation filter 24 and the interpolation bandpass filter within the interpolation unit 26 require high calculation power.

Therefore, all described stereo demultiplexers have the particular disadvantage

that a quite high calculation power is needed.
Therefore, it is the object of the present invention to provide a stereo demultiplexer needing less calculation power.

The stereo demultiplexer according to the present invention is defined in independent claim 1. Preferred embodiments thereof are defined in dependent claims 2 to 9.

According to the present invention the second sampling rate decimation filter, i.e. the sampling rate decimation filter in the sum path, is used for the sampling rate decimation to generate the 2^{nd} harmonic or any other harmonic of the pilot carrier. This sampling rate decimation filter is available anyway and therefore the sampling rate decimation of the pilot carrier can be performed without an additional filter.

The sampling rate of the DPLL output signal needs to be upconverted to a higher sampling rate. Therefore, the sampling rate of the DPLL output signal needs to be interpolated by the same factor D than the sampling rate decimation of the stereo-sum signal.

Preferrably, the sampling rate interpolation of the DPLL output signal is performed in the DPLL without any interpolation filter. In this case the interpolation is achieved on basis of one calculated and D-1 predicted sampling values for the respective harmonic of the pilot carrier. Each of the predicted values is preferrably calculated on basis of a phase correction of the one calculated value which is determined in accordance with the neccessary number of predicted values.

The present invention and its embodiments will be better understood from a detailed description of an exemplary embodiment thereof described in conjunction with the accompanying drawings, wherein

Fig. 1 shows a stereo demultiplexer according to a preferred embodiment of the present invention;

Fig. 2 shows parts of a digital PLL-circuit shown in Fig. 1;

Fig. 3 shows an embodiment of a stereo demultiplexer according to the prior art;

Fig. 4 shows another embodiment of a stereo demultiplexer according to the prior art; and

Fig. 5 shows a further embodiment of a stereo demultiplexer according to the prior art.

Fig. 1 shows a stereo demultiplexer according to a preferred embodiment of the present invention which elucidates the sampling rate decimation. As mentioned above, such a sampling rate decimation according to the present invention can be performed, because the frequency modulated stereo-multiplex signal m(t) has a much higher bandwidth than the frequency demodulated and stereo-demultiplexed audio signal.

As it is shown in Fig. 1, according to the present invention the stereo-sum signal $m_s(t)$ is generated from the stereo-multiplex signal m(t) by a sampling rate decimation with a decimation factor D by a first sampling rate decimation filter 5 which includes a lowpass filter.

The so generated stereo-sum signal $m_s(t)$ is thereafter fed to an adder 3 and a subtracter 6 as described in connection with the stereo demultiplexers shown in Figs. 3 to 5.

According to the present invention also a digital PLL-circuit 4 is working with a decimated sampling rate, but the decimation filtering of the sum path, i.e. the path to generate the stereo-sum signal $m_s(t)$ is used for the sampling rate decimation of the stereo-sum signal $m_s(t)$ and the pilot carrier, i.e. the output signal of the first sampling rate decimation filter 5 is not only input to the adder 3 and the subtracter 6, but also to the DPLL-cicrcuit 4.

In the shown embodiment, the DPLL-circuit 4 generates a carrier for the coherent amplitude demodulation of the stereo-difference signal $m_d(t)$.

As also mentioned above, the coherent amplitude demodulation of the stereo-difference signal $m_d(t)$ needs to be performed at a sampling rate which is

higher than the sampling rate of the audio signal, since the bandwidth of the stereo-multiplex signal m(t) is higher than the bandwidth of the audio signal. Therefore, the carrier for the coherent amplitude demodulation of the stereo-difference signal $m_d(t)$ needs to be generated with a higher sampling rate. Fig. 1 shows that the carrier is generated with a sampling rate that is D times higher than the sampling rate of the stereo-sum signal $m_s(t)$, since the second harmonic of the pilot carrier generated by the DPLL-circuit 4 is interpolated by an interpolation factor of D within the DPLL-circuit 4.

To perform the coherent amplitude demodulation which is necessary to generate the stereo-difference signal $m_d(t)$ the so generated carrier with a carrier frequency of $2\omega_{pil}$ that is locked in phase to the pilot carrier is multiplied with the stereo-multiplex signal m(t) by a demodulator 1 which directly corresponds to the demodulators 1 described in connection with Figs. 3 to 5.

The stereo-difference signal $m_d(t)$ is generated equally as described in connection with Figs. 3 to 5. Therefore, the output signal of the demodulator 1 is sampling rate decimated by a second sampling rate decimation filter 2 which includes a lowpass filter. The so generated stereo-difference signal $m_d(t)$ is fed to an adder 3 and a subtracter 6 as described in connection with the stereo demultiplexers described above in connection with Figs. 3 to 5.

Furtheron, if neccessary, delay elements which equalize the group delay of the first and second sampling rate decimation filters in the sum path and the difference path can be inserted into the stereo-demiultiplexer to achieve that certain signals have the same time relationship.

Additionally to the usage of the decimation filtering of the sum path for the sampling rate decimation of the pilot carrier a further sampling rate decimation can be performed, e.g by a decimation factor of E. In this case also the interpolation factor has to be increased to a value D·E, i.e. so that the recovered pilot carrier has a sampling rate equal to that of the frequency demodulated stereo-multiplex signal m(t).

Fig. 2 shows parts of the digital PLL-circuit 4 in more detail. Basically, the digital PLL-circuit 4 comprises a PLL which outputs a phase signal, a multiplier 13 which multiplies this phase signal with a constant factor which

determines which harmonic of the pilot carrier is to be generated and one or more sinus calculation units which output samples of the reconstructed pilot carrier based on the multiplied phase signal. The number of sinus calculation units determines the interpolation factor.

The PLL itself comprises a first multiplier 7 receiving samples of the stereo-sum signal $m_s(t=1, 2,...) = x(k)$ as multiplicant at a first input, a filter 8 receiving the output signal of said first multiplier 7, a second multiplier 9 multiplying the output signal of the filter 8 with the gain of the phase locked loop, i. e. with a signal PLL_loop_gain, a first adder 11 receiving said output signal of the second multiplier 9 at a first input as a first summand, a constant representing the product of the pilot carrier frequency ω_{pil} and the sampling period T at a second input as a second summand and a delayed phase signal which is the output signal of said first adder 11 at a third input as a third summand, a delay element 12 receiving said phase signal output of said first adder 11 and supplying said delayed phase signal of said first adder 11 to said third input of said first adder 11, and a cosinus calculation unit 10 receiving the phase signal of said first adder 11 and supplying its output signal as multiplier to a second input of said first multiplier 7.

To generate the second harmonic of the pilot carrier the phase signal is multiplied with the constant factor 2 by the third multiplier 13. The output signal of the third multiplier 13 is input to a first sinus calculation unit 14 which transfers the phase signal into a corresponding calculated sample of the second harmonic of the pilot carrier.

To perform an interpolation with an interpolation factor D there is the need that D-1 output samples are aditionally generated based on the phase signal calculated on basis of one input sample x(k). Therefore, one of D-1 phase shift values equally dividing the range to the next expected phase signal, i. e. the phase signal for the input sample x(k+1), is respectively added to the phase signal by a respective one of D-1 adders 16_1 to 16_{D-1} before these generated D-1 phase signals are respectively input to D-1 sinus calculation units 15_1 to 15_{D-1}. These D-1 sinus calculation units respectively output one of D-1 interpolated samples of the second harmonic of the pilot carrier.

The output signals of the first to D^{th} sinus calculation units are sequentially

output as samples of second harmonic of the pilot carrier, i. e. as a signal $y(t=1, 2,...) = y(k/D), y(k/D + 1),..., y(k/D + (D-1))$.

The cosinus calculation unit 10 and the sinus calculation units 14, 15_1 to 15_{D-1} are advantageously realized as look-up tables. Of course, all sinus calculation units 14, 15_1 to 15_{D-1} can be realized as just one sinus calculation unit, since the respective output values are not needed simultaneously.

Claims

1. Stereo demultiplexer receiving a frequency demodulated stereo-multiplex signal (m(t)) which comprises at least a stereo-difference signal ($m_d(t)$), a stereo-sum signal ($m_s(t)$) and a pilot carrier, comprising a PLL-circuit (4) to recover the pilot carrier and/or at least one harmonic thereof to perform an amplitude demodulation, **characterized in that** said PLL-circuit (4) receives the sampling rate decimated stereo-sum signal ($m_s(t)$) as input signal, which is sampling rate decimated by a decimation factor of D.

2. Stereo demultiplexer according to claim 1, **characterized in that** said sampling rate decimated stereo-sum signal ($m_s(t)$) is further sampling rate decimated by a decimation factor of E before said PLL-circuit (4) receives it as input signal.

3. Stereo demultiplexer according to claim 1 or 2, **characterized in that** said PLL-circuit (4) outputs a recovered pilot carrier which is interpolated so that it has a sampling rate equal to that of the frequency demodulated stereo-multiplex signal (m(t)).

4. Stereo demultiplexer according to claim 3, **characterized in that** D-1 or (E·D)-1 interpolated pilot carrier values (y(k/D + 1), ..., y(k/D + (D-1))) and one calculated pilot carrier value (y(k/D)) are alternately output.

5. Stereo demultiplexer according to claim 4, **characterized in that** said interpolation within the PLL-circuit (4) is performed on basis of a prediction starting at said calculated pilot carrier value.

6. Stereo demultiplexer according to claim 5, **characterized by**

- a PLL (7, 8, 9, 10, 11, 12) within the PLL-circuit (4) which outputs a phase signal, and
- a first sinus calculation unit (14) which outputs said one calculated pilot carrier value (y(k/D)) on basis of said phase signal.

7. Stereo demultiplexer according to claim 6, **characterized by**

- second to D^{th} or $(E \cdot D)^{th}$ sinus calculation units (15_1, ..., 15_{D-1}) each of which outputs one of said D-1 or (E·D)-1 interpolated pilot carrier values (y(k/

D + 1), ..., y(k/D + (D-1))) on basis of said phase signal and a respective added phase shift value.

8. Stereo demultiplexer according to claim 6 or 7, **characterized by**

- a third multiplier (13) which multiplies said phase signal with a factor of 2 before it is input to said first sinus calculation unit (14) and/or a respective second to D^{th} or $(E \cdot D)^{th}$ sinus calculation unit (15_1, ..., 15_{D-1}) via a respective second to D^{th} or $(E \cdot D)^{th}$ adder (16_1, ..., 16_{D-1}) which adds said respective phase shift value so that the 2^{nd} harmonic of the pilot carrier is generated.

9. Stereo demultiplexer according to anyone of claims 6 to 8, **characterized in that** said PLL (7, 8, 9, 10, 11, 12) comprises

- a first multiplier (7) receiving samples of the stereo-sum signal (x(k)) as multiplicant at a first input,
- a filter (8) receiving the output signal of said first multiplier (7),
- a second multiplier (9) multiplying said output signal of said filter (8) with a PLL gain (PLL_loop_gain),
- a first adder (11) receiving said output signal of said second multiplier (9) at a first input as a first summand, a constant representing the product of the pilot carrier frequency (ω_{pil}) and the sampling periode(T) at a second input as a second summand, and a delayed phase signal which is the output signal of said first adder (11) at a third input as a third summand,
- a delay element (12) receiving said phase signal of said first adder (11) and supplying said delayed phase signal to said third input of said first adder (11), and
- a cosinus calculation unit (10) receiving the phase signal of said first adder (11) and supplying its output signal as multiplier to a second input of said first multiplier (7).

Abstract

Digital stereo demultiplexer

In a stereo demultiplexer receiving a frequency demodulated stereo-multiplex signal (m(t)) which comprises at least a stereo-difference signal ($m_d(t)$), a stereo-sum signal ($m_s(t)$) and a pilot carrier, a PLL-circuit (4) to recover the pilot carrier and/or at least one harmonic thereof receives the sampling rate decimated stereo-sum signal ($m_s(t)$) as input signal, which is sampling rate decimated by a decimation factor of D. Therefore, the sampling rate decimation filter in the sum path is used for the sampling rate decimation to generate the 2^{nd} harmonic or any other harmonic of the pilot carrier. This sampling rate decimation filter is available anyway and therefore the sampling rate decimation of the pilot carrier can be performed without an additional filter.

(Fig. 1)

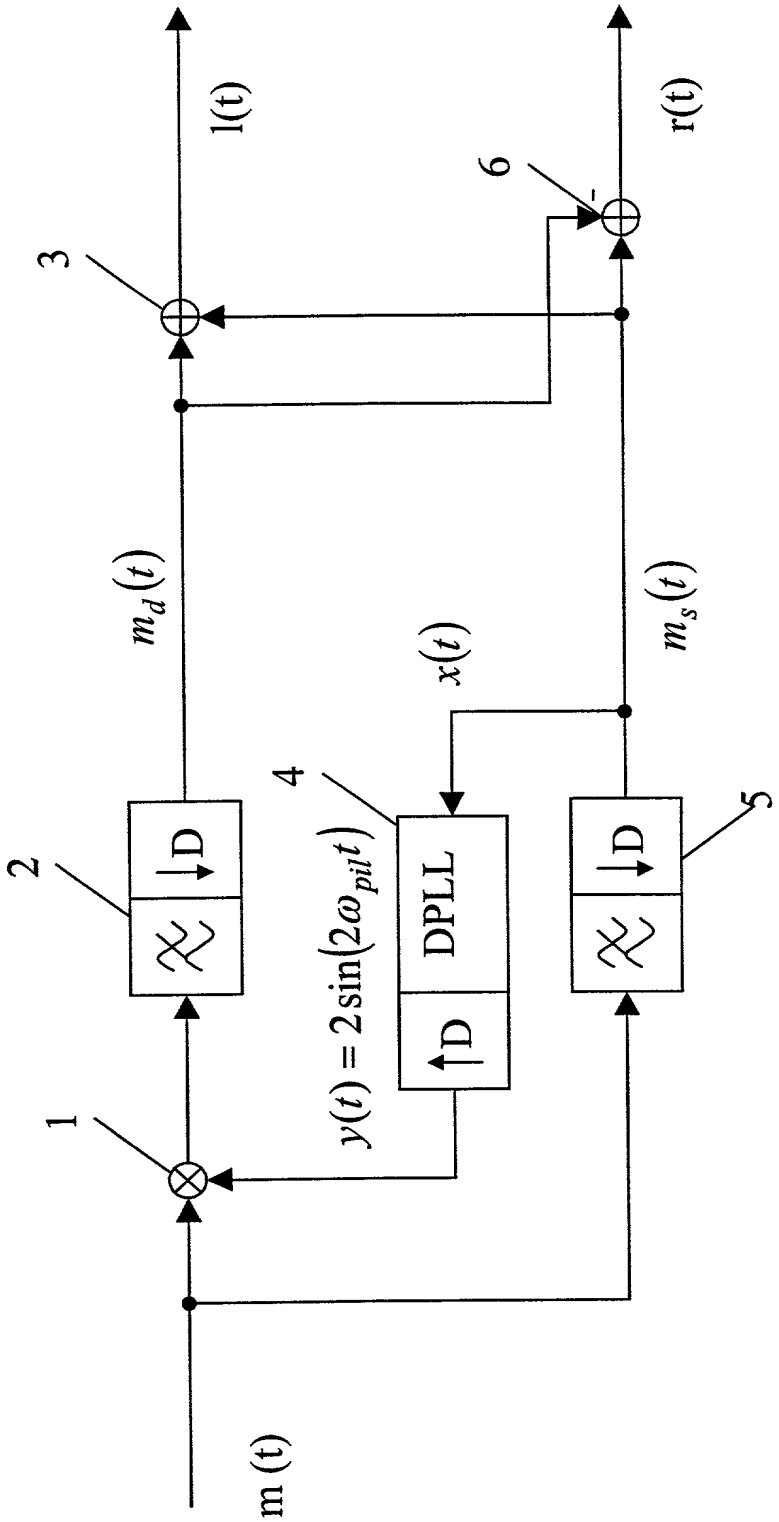
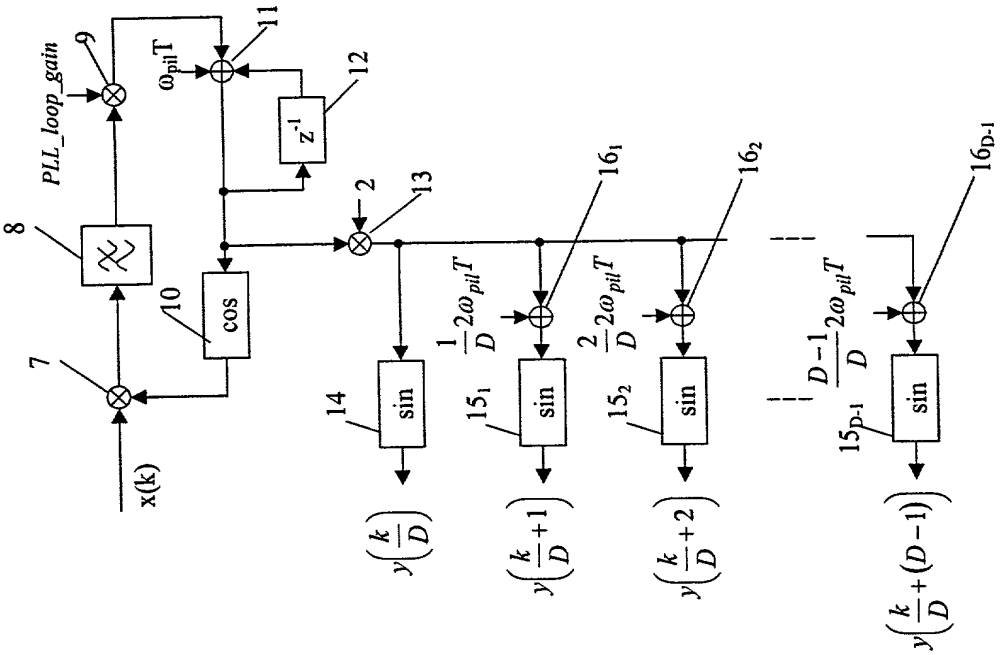


Figure 1

Figure 2


x(k)
7
8
PLL_loop_gain
9
cos
10
$\omega_{pil}T$
11
z^{-1}
12
2
13
14
sin
$y\left(\frac{k}{D}\right)$
$\frac{1}{D}2\omega_{pil}T$
15_1
16_1
$y\left(\frac{k}{D}+1\right)$
$\frac{2}{D}2\omega_{pil}T$
15_2
16_2
$y\left(\frac{k}{D}+2\right)$
$\frac{D-1}{D}2\omega_{pil}T$
15_{D-1}
16_{D-1}
$y\left(\frac{k}{D}+(D-1)\right)$

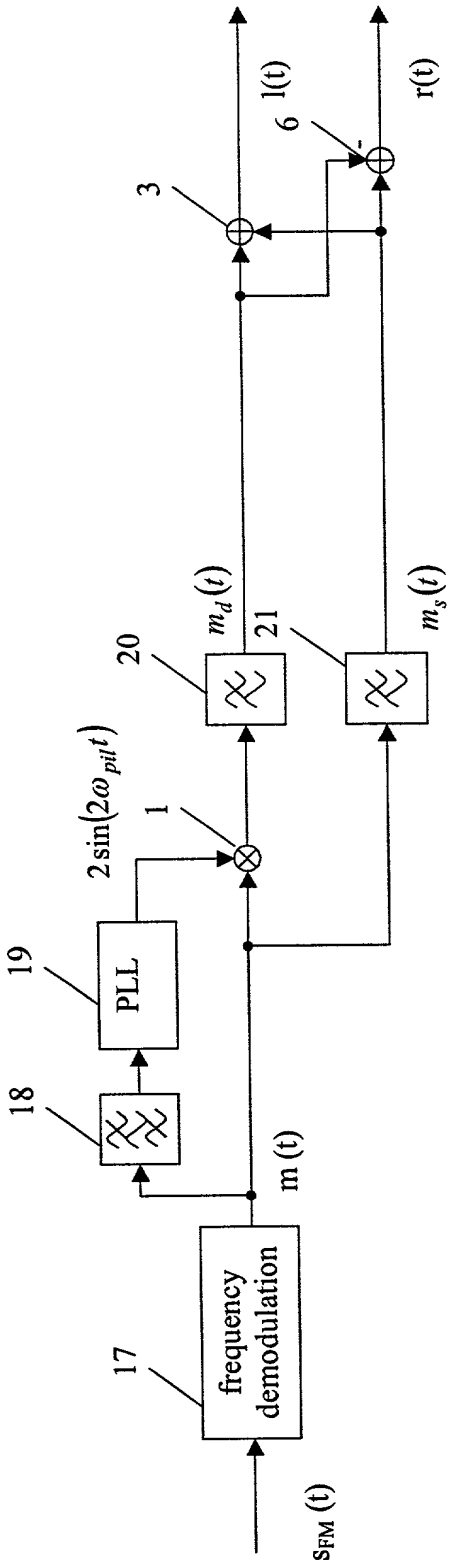

frequency demodulation
17
s_{FM} (t)
m (t)
18
19
PLL
$2\sin(2\omega_{pil}t)$
1
20
21
$m_d(t)$
$m_s(t)$
3
6
l(t)
r(t)

Figure 3

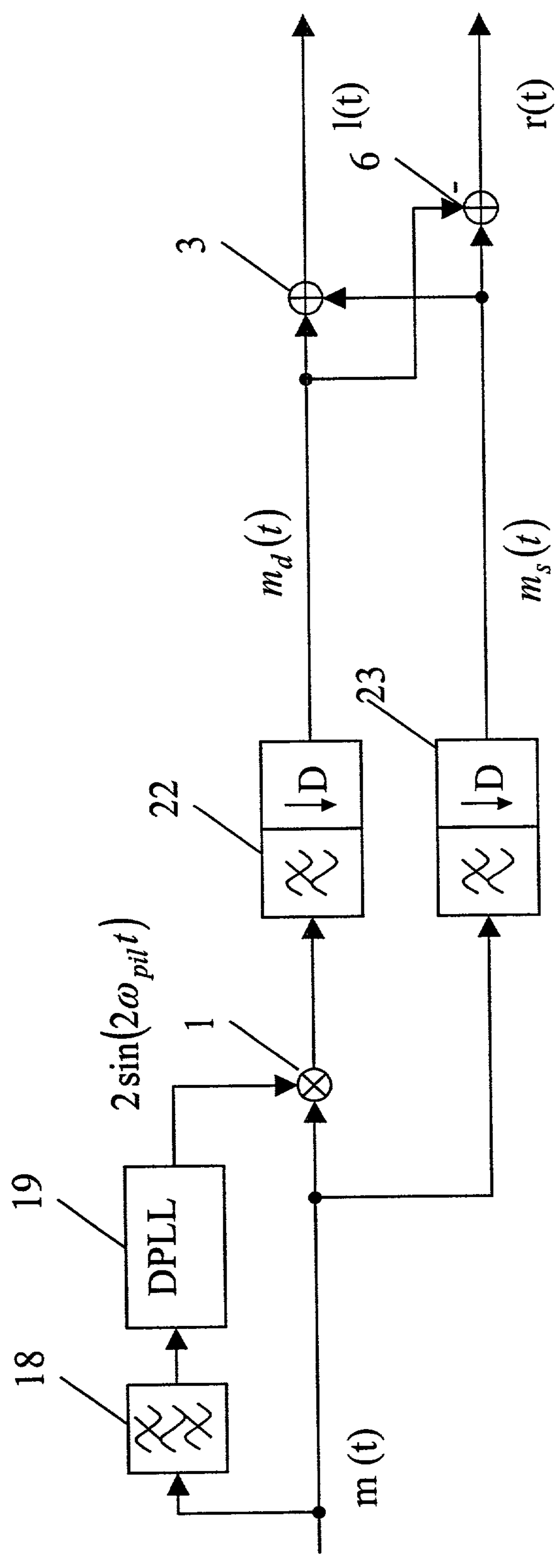


Figure 4

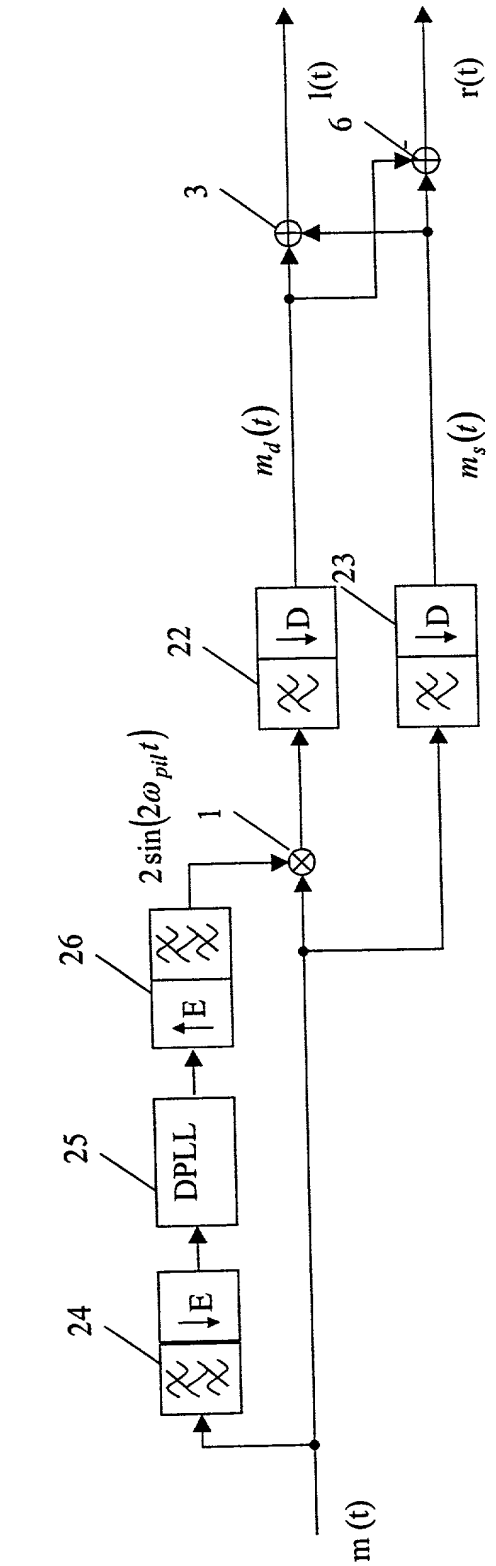


Figure 5

DECLARATION FOR PATENT APPLICATION (JOINT OR SOLE)
(Under 37 CFR § 1.63; with Power of Attorney)
FROMMER LAWRENCE & HAUG LLP

FLH File No. 450117-02749

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention ENTITLED:

DIGITAL STEREO DEMULTIPLEXER

the specification of which

__X__ is attached hereto.

_____ was filed on _____ as Application Serial No. _____,

with amendment(s) through _____ (if applicable, give dates).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) [list additional applications on separate page]:			Priority Claimed:	
Number:	Country:	Filed (Day/Month/Year):	Yes	No
99 120 798.6	Europe	20 October 1999	X	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Application(s) [list additional applications on separate page]:		
Appln. Ser. Number:	Filed (Day/Month/Year):	Status (patented, pending, abandoned):

I hereby appoint WILLIAM S. FROMMER, Registration No. 25,506, and DENNIS M. SMID, Registration No. 34,930 or their duly appointed associate, my attorneys, with full power of substitution and revocation, to prosecute this application, to make alterations and amendments therein, to file continuation and divisional applications thereof, to receive the Patent, and to transact all business in the Patent and Trademark Office and in the Courts in connection therewith, and specify that all communications about the application are to be directed to the following correspondence address:

WILLIAM S. FROMMER, Esq.
c/o FROMMER LAWRENCE & HAUG LLP
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New York, New York 10151

Direct all telephone calls to:
(212) 588-0800
to the attention of:
WILLIAM S. FROMMER

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

INVENTOR(S):

Signature: _____ Date: _____

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Residence: Weinstadt, Germany
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Signature: _____ Date: _____

Full name of 2nd joint inventor (if any):
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[Similarly list additional inventors on separate page]

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Note: In order to qualify for reduced fees available to Small Entities, each inventor and any other individual or entity having rights to the invention must also sign an appropriate separate "Verified Statement (Declaration) Claiming [or Supporting a Claim by Another for] Small Entity Status" form [e.g. for Independent Inventor, Small Business Concern, Nonprofit Organization, individual Non-Inventor].

Note: A post office address must be provided for each inventor.